ISSN: 2277-9655
Scientific Journal Impact Factor: 3.449
(ISRA), Impact Factor: 2.114

IJESRT

INTERNATIONAL JOURNAL OF ENGINEERING SCIENCES & RESEARCH TECHNOLOGY

Energy Aware FSM Based Architecture for Matching of Data Encoded With Error-Correcting Codes: Survey

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Abstract

A new architecture for matching the data protected with an error-correcting code (ECC) is presented in this brief to reduce latency and complexity. In this paper, by making use of the property that soft errors are rare and hard errors increase gradually with the number of writes, a novel scheme is proposed to correct both soft and hard errors through integrating 2-error-correcting BCH codes and ECPs (error-correcting pointers). In particular, we propose an efficient technique for partial self-checking FINITE STATE MACHINES (FSM) design based on on-line monitoring of FSM state transitions.

Introduction

Data comparison circuit is a logic that has many applications in a computing system. Another place that uses a data comparison circuit is in the translation look-aside buffer (TLB) unit. TLB is used to speed up virtual to physical address translation. Error correcting codes (ECC) are widely used in modern microprocessors to enhance the reliability and data integrity of their memory structures.

As recent computers employ error-correcting codes (ECCs) to protect data and improve reliability complicated decoding procedure, which must precede the data comparison, elongates the critical path and exacerbates the complexity overhead. The direct compare method which encodes the incoming data and then compares it with the retrieved data that has been encoded as well. Therefore, the method eliminates the complex decoding from the critical path.

This paper provides an overview of the the retrieved data resides in the error correctable range of the codeword corresponding to the incoming data. As the checking necessitates an additional circuit to compute the Hamming distance, i.e., the number of different bits between the two codewords, the saturate adder (SA) was presented as a basic building block for calculating the Hamming distance. Therefore, the latency and the hardware complexity are decreased considerably even compared with the SAbased architecture.

Literature survey

Wei, Dinesh and Shih [1] proposed a computing system where incoming information needs to be compared with a piece of stored data to locate the matching entry, e.g., cache tag array lookup and translation look-aside buffer matching. If the stored data is protected with error-correcting codes (ECC) for reliability reason, the previous solution is to access the stored information, decode and correct if necessary before it is used to compare with the incoming data. The decoding and correcting step increases the total access time, which is often critical. They proposed a method to improve the compare latency for information encoded with ECC and used the cache tag array look-up as an example, and results show that less gate count reduction and latency reduction are achieved. The new approach saves roughly 35% and 30% in total gate counts. With lower gate count and less area, the routing and interconnect complexity should be lower resulting in smaller routing area and shorter routing latency.

Lee, Yoo and Park [2] proposed, Solid-state drives (SSDs), built with many flash memory channels, is usually connected to the host through an advanced high-speed serial interface such as SATA III associated with a transfer rate of 6Gb/s. However, the performance of SSD is in general determined by the throughput of the ECC blocks necessary to overcome the high error-rate. The binary BCH code is widely used for the SSD due to its powerful error-correction

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capability. As it is hard to achieve high-throughput strong BCH decoders, multiple BCH decoders are typically on a high-performance SSD controller, leading to a significant increase of hardware complexity. They presented an efficient BCH encoder/decoder architecture achieving a decoding throughput of 6Gb/s. The overall architecture includes a single BCH decoder and a multi-threaded BCH encoder. The single BCH encoder is responsible for all the channels and services a channel at a time in a round-robin manner.

Warnock, Chan and Wen [3] proposed the circuit and physical design features of the z196 processor chip, implemented in a 45 nm SOI technology. The chip contains 4 super-scalar, out-of-order processor cores, running at 5.2 GHz, on a die with an area of 512 mm containing an estimated 1.4 billion transistors. The core and chip design methodology and specific design features are presented, focusing on techniques used to enable high-frequency operation. In addition, chip power, IR drop, and supply noise are discussed, being key design focus areas. The chip's ground-breaking RAS features are also described, engineered for maximum reliability and system stability. The z196 chip was designed to push frequency and performance to new limits, using unique features in the 45 nm technology, tools and methods optimized for high-frequency design, and a variety of special circuits in key critical areas. At the chip level, a focus on power, IR drop, and supply noise were all key enablers of this high-performance design. These design goals were met while simultaneously adding new RAS features to the design, starting from the base circuit level and proceeding up to the system level, all without sacrificing the RAS features introduced in previous design. This combination of industry-leading RAS and unprecedented chip frequency allows the z-Enterprise system to reach new levels of performance and stability for the most critical workloads.

Tremblay and Chaudhry [4] proposed, the Chip-Multithreading (CMT) SPARC processor consists of 16 cores with shared memory architecture and supports a total of 32 main threads plus 32 scout threads. It is targeted for high-performance servers, and is optimized for both single- and multi-threaded applications. The 396 mm chip is fabricated in an 11 metal layer 65-nm CMOS process and operates at a nominal frequency of 2.3 GHz, consuming a maximum power of 250W at 1.2 V. It provides an overview of the architectural highlights and describes the physical implementation challenges and solutions including circuit innovations in memory arrays, register files, and floating-point hardware that boost the performance and circuit robustness with low area overhead. This chip-multithreading (CMT) SPARC processor is targeted for high-performance servers and is optimized for both single- and multi-threaded applications. This required the development of a new pipeline architecture that addresses both the performance and scalability issues as well as the physical challenges of multi-core design.
Physical implementation of the design boost performance and robustness, while at the same time minimize chip area, design effort, and time.

Chang, chen, Chiu and Rusu [5] proposed a single-ported 16-MB cache for the Dual-Core Intel Xeon Processor 7100 Series uses a 0.624 m2 cell in a 65-nm 8-metal technology. Low power techniques are implemented in the L3 cache to minimize both leakage and dynamic power. Sleep transistors are used in the SRAM array and peripherals, reducing the cache leakage by more than 2X. Only 0.8% of the cache is powered up for a cache access. Dynamic cache line disable (Intel Cache Safe Technology) with a history buffer protects the cache from latent defects and infant mortality failures. An on-die history table (Pellston Queue) keeps track of random ECC events for each cache line. The first time an ECC error occurs on a cache line it could be a soft-error. The second occurrence of ECC error to the same location means that it is less likely to be a soft-error, but more likely a physical issue. Cache Safe Technology is enabled during both power-on self-test and in normal operation. Long channel length devices are used to further reduce the leakage power consumption. A shutdown option is implemented in the SRAM arrays to minimize the leakage power for the inactive sub-arrays. Aggressive clock gating, fine-grained sleep resolution, and wake-up counters were implemented to minimize the dynamic power.

Ando, Yosida and Morita [6] proposed a fifth-generation SPARC64 processor is fabricated in 130-nm partially depleted silicon-on-insulator CMOS with eight layers of Cu metallization. The 16-byte-wide system bus operates with a 260-MHz clock in single-data-rate or double-data-rate modes. This processor implements an error-detection mechanism for execution units and data path logic circuits in addition to on-chip arrays to detect data corruption. Intermittent errors detected in execution units and data paths are recovered via instruction retry. A soft barrier clocking scheme allows amortization of the clock skew and jitter over multiple cycles and helps

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to achieve high clock frequency. Tunability of the clock timing makes timing closure easier. A relatively small amount of custom circuit design and the use of mostly static circuits contributes to achieve short development time. Improving performance without consuming too much power was another important goal of this processor development. The target was to achieve twice the performance with equal or less power compared with the fourth-generation SPARC64 processor, which runs at 563 MHz and consumes about 50 W (0.18- m technology, 1.8-V). To achieve this goal, a new 130-nm partially depleted silicon-on-insulator (SOI) CMOS process was selected. Minimizing the risk of using the new semiconductor process and keeping the design on schedule were also important considerations.

Conclusion

In this work, it has been concluded that a new architecture has been presented for matching the data protected with an ECC. In addition, an efficient processing architecture has been presented to further minimize the latency and complexity. As the proposed architecture is effective in reducing the latency as well as the complexity considerably, it can be regarded as a promising solution for the comparison of ECC-protected data.

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